REMARKS

Examiner C. Young, is thanked for the thorough examination and search of the subject Patent Application. Claims 20 and 24 have been amended. Claims 1-19 have been canceled due to a restriction requirement that has been made final.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of Claims 20-27 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention, is requested based on Amended Claims 20 and 24 and on the following remarks.

Applicant has amended Claims 20 and 24 to make clear the metes and bounds of the method. Amended Claim 20 now reads:

20. (Currently Amended) A method to pattern a photoresist layer in the manufacture of an integrated circuit device wherein said integrated circuit device comprises a plurality of fields, said method comprising:

depositing a photoresist layer overlying a wafer;

loading a first mask and a second mask in a mask stage of an exposure apparatus wherein said mask stage maintains a fixed relative position between said first mask and said second mask;

aligning said first mask and said second mask to said wafer;

indexing said wafer ~~to~~ such that said first mask overlies a starting said field; ~~to set a current field;~~

~~thereafter scanning said first mask to expose said current field;~~

~~thereafter stepping said wafer to a next field unexposed by said first mask to set a new said current field;~~

~~thereafter repeating said scanning and stepping until every said field on said semiconductor substrate is exposed with said first mask;~~

thereafter performing a first exposure pass on said wafer by repeatedly performing the steps of:

scanning said field using said first mask; and

stepping said wafer such that said first mask overlies a next said field yet unexposed by said first mask;

until all said fields in said wafer have been exposed by said first mask;

thereafter ~~returning~~ indexing said wafer ~~to~~ such that said second mask overlies said starting field; ~~to set said current field;~~

~~thereafter scanning said second mask to expose said current field;~~

~~thereafter stepping said wafer to a next field unexposed by said second mask to set a new said current field;~~

~~thereafter repeating said scanning and stepping until every said field on said semiconductor substrate is exposed with said second mask to thereby superimpose the patterns of said first mask and said second mask in every said field; and~~

thereafter performing a second exposure pass on said wafer by repeatedly performing the steps of:

scanning said field using said second mask; and

stepping said wafer such that said second mask overlies a next said field yet unexposed by said second mask;

until all said fields in said wafer have been exposed by said second mask; and

developing said photoresist layer to thereby complete said patterning in the manufacture of said integrated circuit device.

Several features of Amended Claim 20 shall be noted. First, lines 3-4 add the phrase wherein said integrated circuit device comprises a plurality of fields to make clear that the wafer surface area is divided into a large array of fields 404 as shown in Fig. 9. In lines 10-11, the phrase "aligning said first mask and said second mask to said wafer" is amended to make clear that a single alignment is performed for the entire scanning method of Claim 20. The fact that the first and second masks are held in fixed arrangement allows the first mask to be used to expose every field 404 during the first pass (Fig. 9) and the second mask to be used to expose every field 404 during the second pass (Fig. 10) without a time consuming mask change and re-alignment (second paragraph, page 14 of Specification). Claim 20 has been amended to make clear the recitation of the first exposure pass (lines 22-29) and the second exposure pass (lines 44-50).

Amended Claim 24 now reads:

24. (Currently Amended) A method to pattern a photoresist layer in the manufacture of an integrated circuit device wherein said integrated circuit device comprises a plurality of fields, said method comprising:

depositing a photoresist layer overlying a wafer;

loading a first mask and a second mask in a mask stage of an optical lithographic, stepper wherein said mask stage maintains a fixed relative position between said first mask and said second mask;

aligning said first mask and said second mask mask to said wafer;

indexing said wafer ~~to~~ such that said first mask overlies a starting field; ~~to set a current field;~~

~~thereafter scanning said first mask to expose said current field;~~

~~thereafter scanning said second mask to expose an adjacent field;~~

~~thereafter stepping said wafer to a next field unexposed by said first mask to set a new said current field; and~~

~~thereafter repeating said scanning and stepping until every said field on said semiconductor substrate is exposed;~~

thereafter performing a first exposure pass on said wafer by repeatedly performing the steps of:

scanning said field using said first mask;

scanning an adjacent field using said second mask; and

stepping said wafer such that said first mask overlies a next said field yet unexposed by said first or second masks;

until all said fields in said wafer have been exposed by either said first mask or said second mask;

thereafter ~~returning~~ indexing said wafer ~~to~~ such that said first mask overlies said starting field; ~~to set said current field;~~

~~thereafter stepping said wafer to a next field unexposed by said second mask to set a new said current field;~~

~~thereafter scanning said second mask;~~

~~thereafter stepping said wafer to a next field unexposed by said first mask to set a new said current field;~~

~~thereafter scanning said first mask to expose said current field;~~

~~thereafter repeating said scanning and stepping until every said field on said semiconductor substrate is exposed to thereby superimpose the patterns of said first mask and said second mask in every said field; and~~

thereafter performing a second exposure pass on said wafer by repeatedly performing the steps of:

stepping said wafer such that said second mask

overlies a next said field yet unexposed by said second mask;

scanning said field using said second mask;

stepping said wafer such that said first mask overlies a next said field yet unexposed by said first mask; and

scanning said field using said first mask;

until all said fields in said wafer have been exposed by said first mask and by said second mask; and

developing said photoresist layer to thereby complete said patterning in the manufacture of said integrated circuit device.

The above-described amendments to Claim 20 have been made to Claim 24. These amendments specify the plurality of fields on the wafer (lines 3-4), the alignment step (lines 10-11), and the first and second exposure passes (lines 24-33 and lines 50-61, respectively). In addition, Claim 24 has been amended to clarify the features of the claimed invention as corresponding to the second embodiment, described in the original application, pages 20-22 and Figs. 11-13. In particular, the first exposure pass (lines 24-33) corresponds to Fig. 12 with the features scanning a first field with the first mask and an adjacent field with the second mask, then stepping to a new (non-exposed) field and

repeating the process until each field has been exposed by either the first of second mask as shown. The second exposure pass (lines 50-61) corresponds to Fig. 13 with the features of stepping to locations not exposed by the second mask and exposing by the second mask at these locations as well as stepping to locations not exposed by the first mask and exposing by the first mask at these locations.

Applicant believes that the above-described amendments to Claims 20 and 24 should meet the requirement, under 35 U.S.C. 112, second paragraph, by providing a recitation that is definite by particularly pointing out and distinctly claiming the subject matter which applicant regards as the invention. Claims 21-23 and 25-27 represent patentably distinct, further limitations on Claim 20 and 24 and should be within the requirements of 35 U.S.C. 112, second paragraph, with the entrance of Amended Claims 20 and 24.

Reconsideration of Claims 20-27 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention, is requested based on Amended Claims 20 and 24 and on the above remarks.

Applicants have reviewed the prior art made of record and not relied upon and have discussed their impact on the present invention above.

Allowance of all Claims is requested.

It is requested that should the Examiner not find that the Claims are now Allowable that the Examiner call the undersigned at 989-894-4392 to overcome any problems preventing allowance.

Respectfully submitted,

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